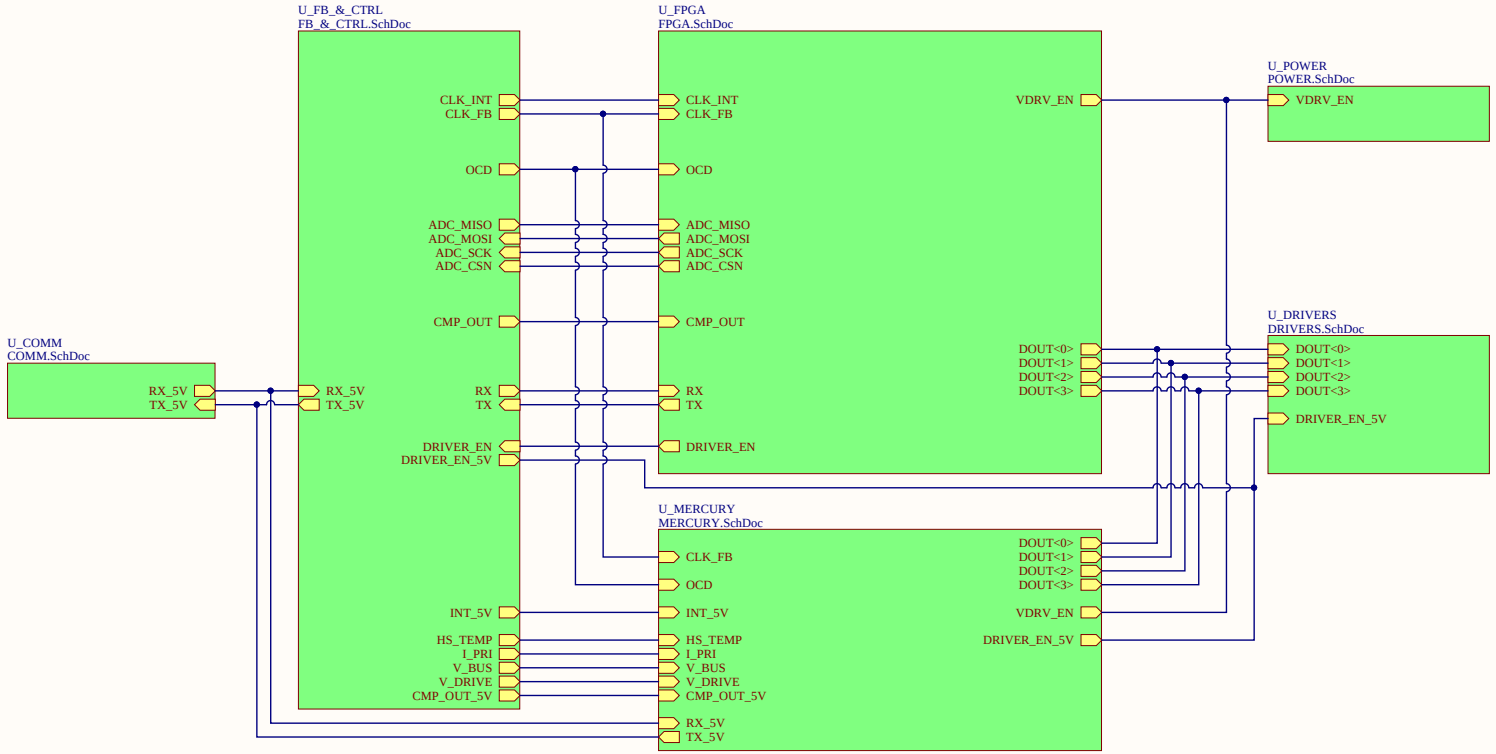
REV	DESCRIPTION	DATE	REVISED BY
1	INITIAL DESIGN	02/03/2018	M LEWIS



Title	*FPGA DRSSTC CONTROLLER*		
Size: B	Number: VMC18-01	Revision: 1	
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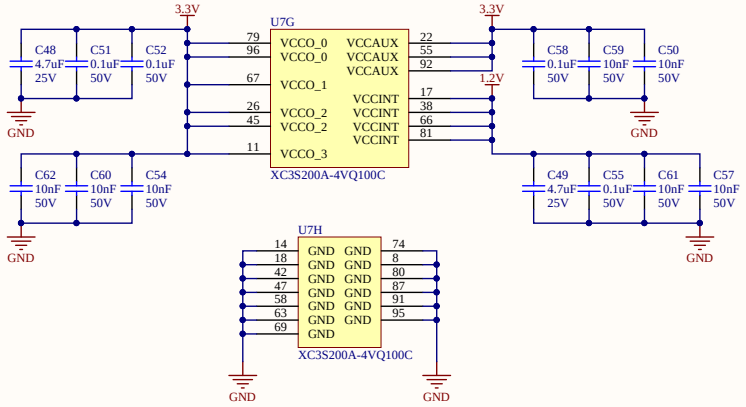
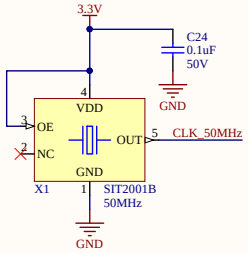
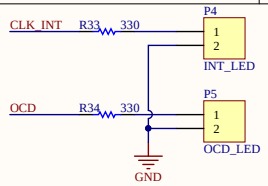


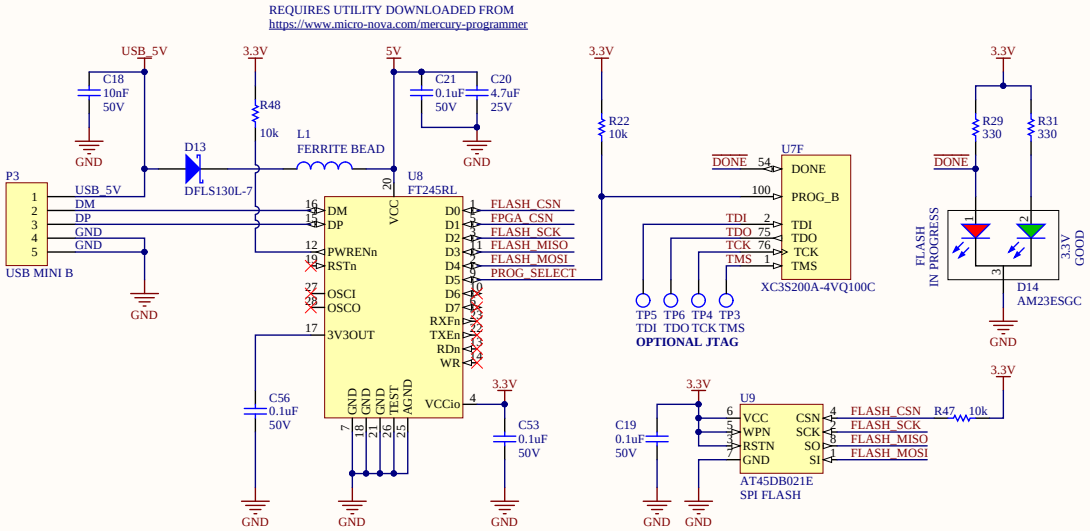
FPGA POWER PINS



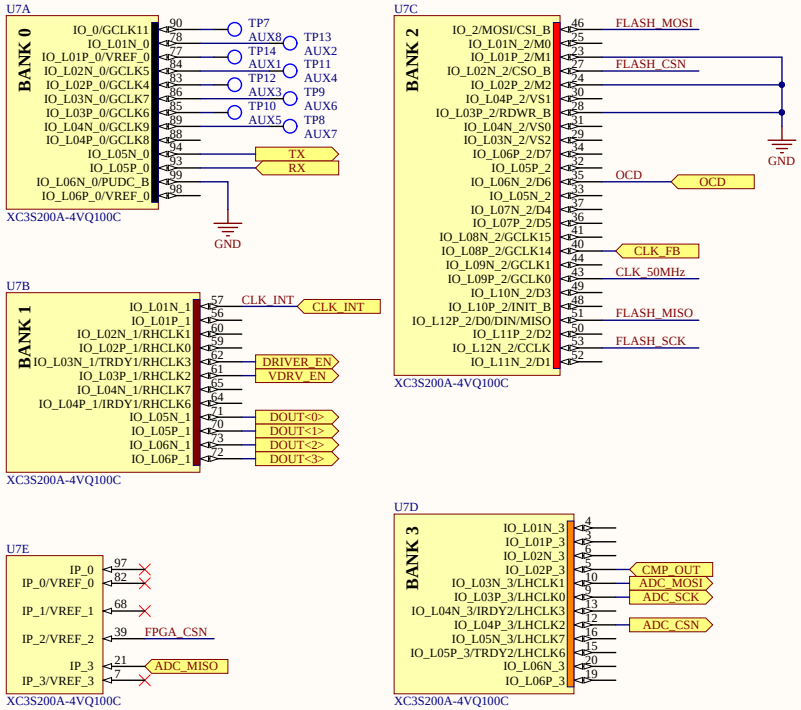
50MHZ OSCILLATOR



INDICATOR LEDS



FPGA PROGRAMMING/SPI FLASH



FPGA I/O

NOTE: FPGA SUPPORT CIRCUITRY DESIGN BORROWED FROM MICRONOVA MERCURY BOARD.
PLEASE VISIT https://www.micro-nova.com/mercury/ FOR MORE INFORMATION

Title	*FPGA DRSSTC CONTROLLER*		
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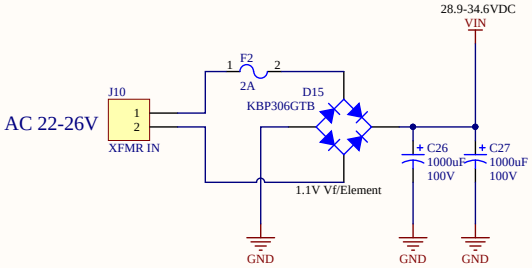
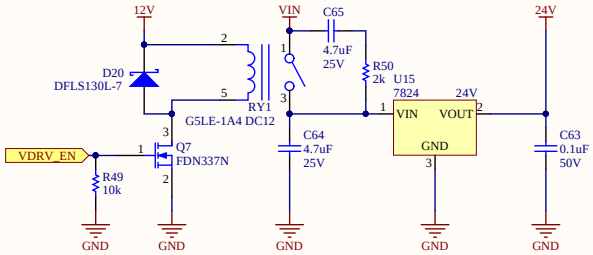
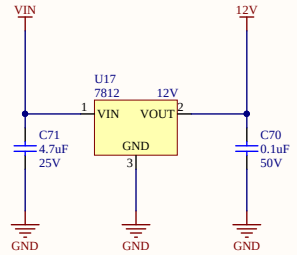


AC/DC SUPPLY



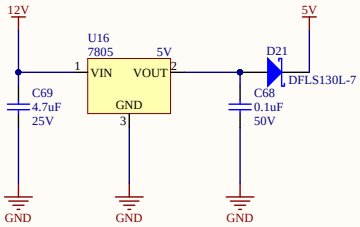
24V SUPPLY

REQUIRES HEAT SINK
GATE DRIVE POWER



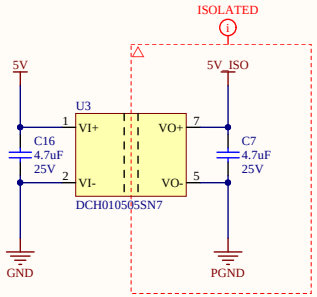
12V SUPPLY

REQUIRES HEAT SINK
GENERIC POWER



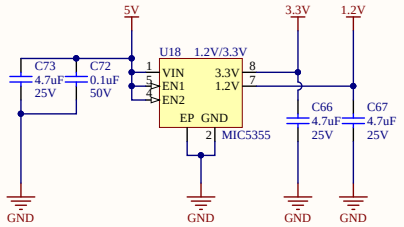
5V SUPPLY

REQUIRES HEAT SINK
DIGITAL LOGIC POWER



ISOLATED 5V SUPPLY

BUS MEASUREMENT POWER



3.3V/1.2V SUPPLY

FPGA I/O/CORE POWER

Title	FPGA DRSSTC CONTROLLER		
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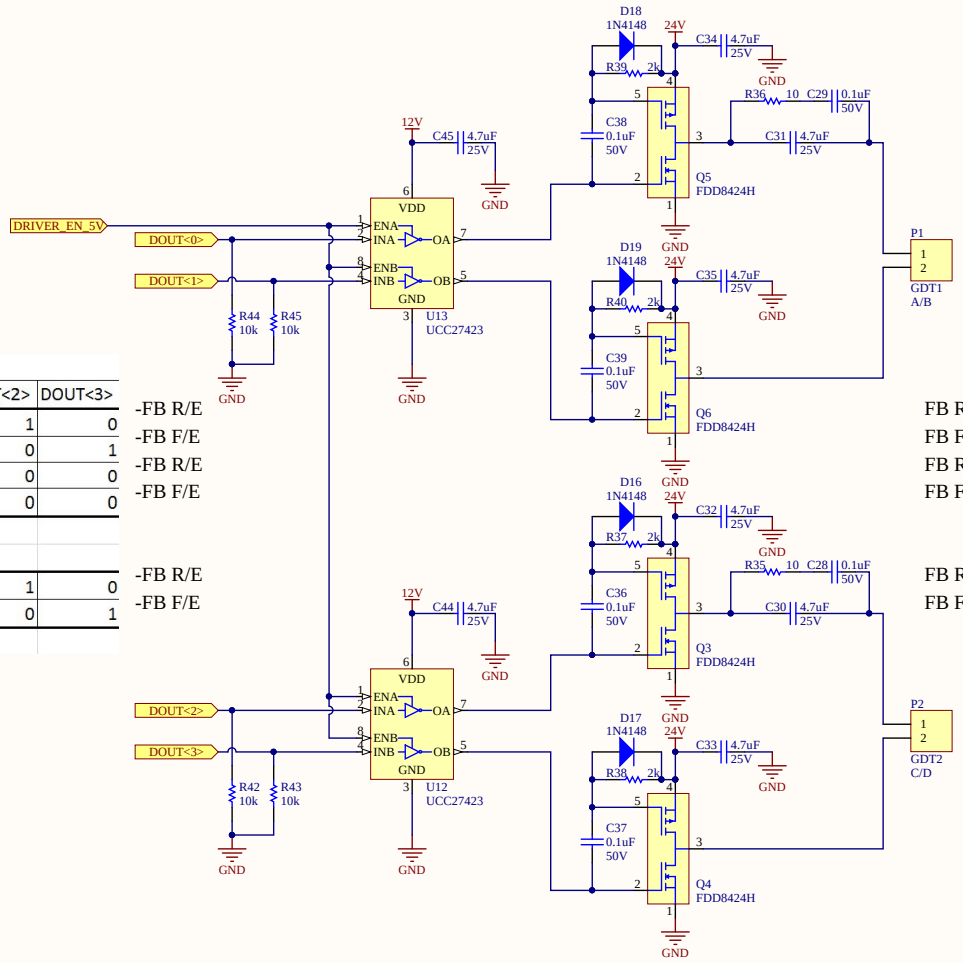
PIN LOGIC

	PINS			
STATE	DOUT<0>	DOUT<1>	DOUT<2>	DOUT<3>
1	0	0	1	0
2	0	0	0	1
3	0	1	0	0
4	1	0	0	0
FREEWHEELING MODE				
5	0	1	1	0
6	1	0	0	1
STANDARD MODE				

-FB R/E
-FB F/E
-FB R/E
-FB F/E

-FB R/E
-FB F/E



FB R/E-
FB F/E-
FB R/E-
FB F/E-

FB R/E-
FB F/E-

GATE LOGIC

	GATES			
STATE	A	B	C	D
1	0	0	0	1
2	0	0	1	0
3	0	1	0	0
4	1	0	0	0
FREEWHEELING MODE				
5	0	1	0	1
6	1	0	1	0
STANDARD MODE				

GATE ORIENTATION

A D

B C

GATE DRIVE TRANSFORMER CONTROL

Title	FPGA DRSSTC CONTROLLER		
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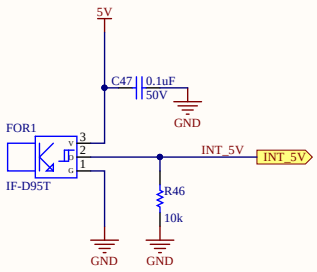
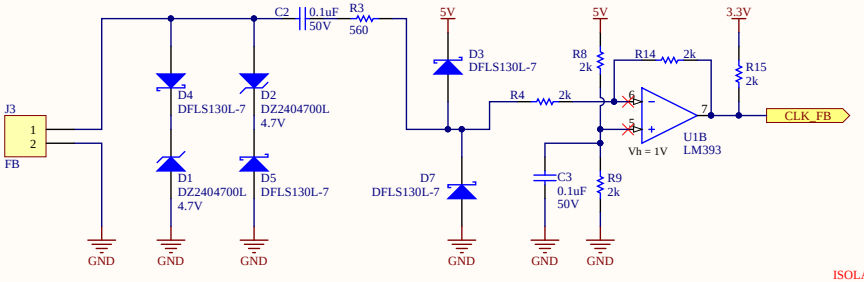
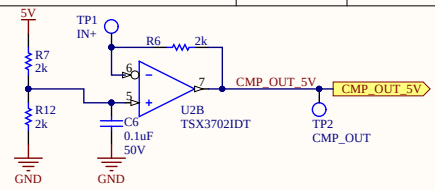


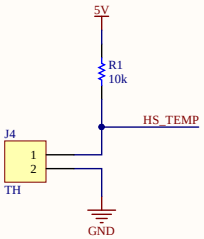
INTERRUPTER INPUT



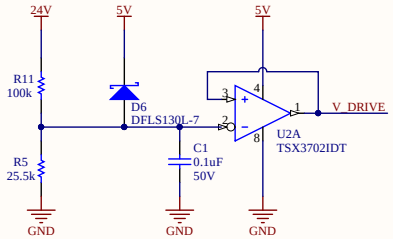
FEEDBACK CLEANUP



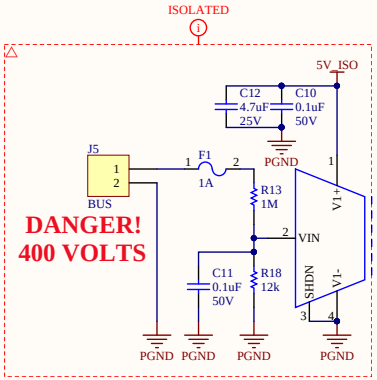
SPARE COMPARATOR

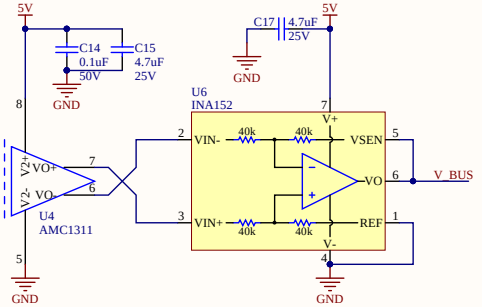


HEATSINK TEMP MEASURE

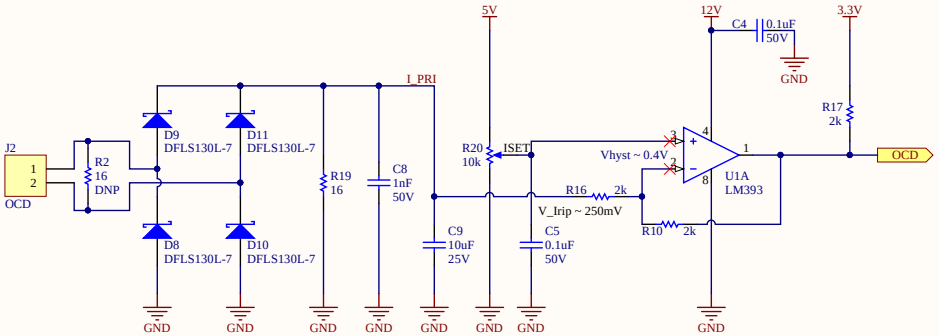


DRIVE VOLTAGE MEASURE

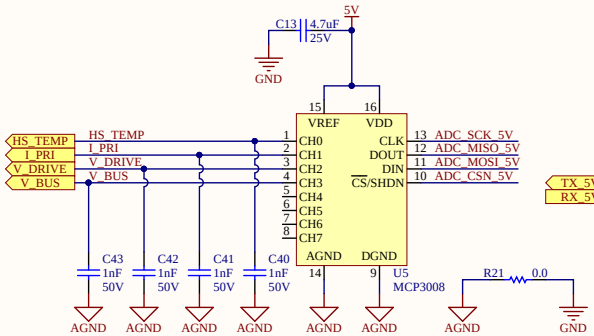




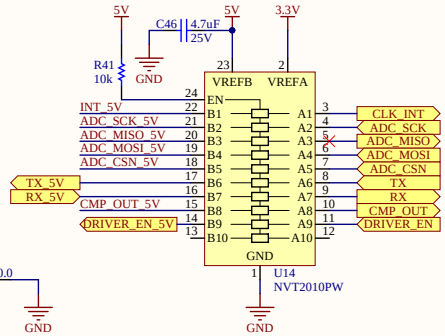
BUS VOLTAGE MEASURE



OVER-CURRENT DETECTION



ANALOG/DIGITAL CONVERTER



LEVEL SHIFTER 5V/3.3V

Title	FPGA DRSSTC CONTROLLER		TEK15 SOLUTIONS
Size: B	Number: VMC18-01	Revision: 1	M LEWIS
Date: 6/25/2018		Sheet 5 of 7	(c) FEBRUARY 2018
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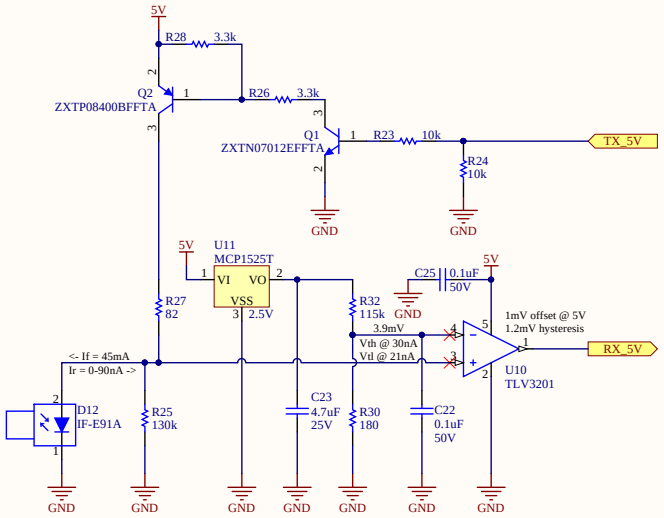
REV	DESCRIPTION	DATE	REVISED BY
1	INITIAL DESIGN	02/03/2018	M LEWIS



BIDIRECTIONAL FIBER OPTIC COMMUNICATION

Title	FPGA DRSSTC CONTROLLER		
Size: B	Number: VMC18-01	Revision: 1	
Date: 6/25/2018		Sheet 6 of 7	
File: COMM.SchDoc			

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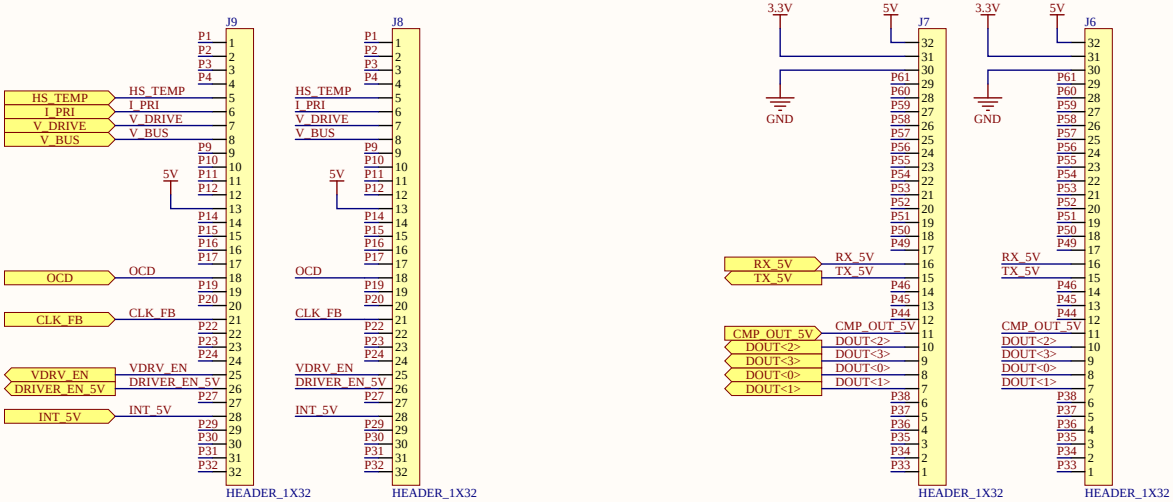
1	INITIAL DESIGN	02/03/2018	M LEWIS



MICRONOVA MERCURY BOARD SOCKETS

Title	*FPGA DRSSTC CONTROLLER*		
Size: B	Number: VMC18-01	Revision: 1	
Date: 6/25/2018		Sheet 7 of 7	
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